CW32 Series MCU Pre-Mass Production Checklist

Application note

Introduction

This document provides recommendations for mass production of designs based on the CW32 family of microcontrollers and can also be used as a reference document when debugging new designs.

- Chapter 1 describes the hardware configuration requirements that must be attended to before mass production of MCUs

- Chapter 2 describes the software configuration requirements that must be attended to before mass production of MCUs

- Chapter 3 describes the production-related requirements that must be attended to before mass production of MCUs

This document is only intended as a reference document for design and mass production and does not fully cover all requirements related to mass production configuration. Before you start, please read carefully the user manual and datasheet for the MCU you are using and more information can be found at *www.whxy.com*.

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1 Hardware checklist

Before mass production of designs based on the CW32 family of microcontrollers, the hardware-related configuration must be checked, as shown in the following table:

Table 1-1 Hardware configuration requirements

Item	Requirements	Remarks
BOOT pin	The BOOT pin should be grounded through a 10KΩ resistor	BOOT=0, Main Flash memory is selected as boot area; BOOT=1, Bootloader memory is selected as boot area.
Programmer ports	The programmer ports should be retained	The minimum programmer ports are: VCC-GND-SWCLK-SWDIO. The maximum programmer ports are: VCC-GND-SWCLK-SWDIO-BOOT-NRST. If using CW-DAPLINK, it should be noted that 1. the VTREF pin of CW-DAPLINK must always be connected to VCC; 2. CW-DAPLINK can supply 3.3V to the target board; 3. For non-3.3V systems, the target board must be powered separately and the VDD pin of the CW-DAPLINK can be left unconnected.
LSE	The distance between the crystal and the LSE pins should be as short as possible	When calculating the matching capacitance, the parasitic capacitance of the PCB should be taken into account of approximately 3 ~ 6pF; Crystal matching service is available by contacting the crystal manufacturer.
LSE	The power supply and ground of the crystal should be treated separately	
LSE	The crystal and external signals should reduce mutual interference	
LSE	The load capacitance and drive power of the crystal should be in accordance with the requirements of the crystal manual	
HSE	The distance between the crystal and the HSE pins should be as short as possible	When calculating the matching capacitance, the parasitic capacitance of the PCB should be taken into account of approximately 3 ~ 6pF; Crystal matching service is available by contacting the crystal manufacturer.
HSE	The power supply and ground of the crystal should be treated separately	
HSE	The crystal and external signals should reduce mutual interference	
HSE	The load capacitance and drive power of the crystal should be in accordance with the requirements of the crystal manual	

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Item	Requirements	Remarks
ADC	VDDA/VDD/VSSA/VSS should be separated to improve ADC accuracy	
	Additional capacitors should be added next to the channel pins to be sampled to improve ADC accuracy	
	External reference voltage should be used if the accuracy of Internal reference voltage does not meet the application requirements	
GPIO	Input voltage to GPIO should be no greater than V_{CC}+0.3V	No 5V tolerant I/O, input voltage forbidden to be greater than V_{CC}+0.3V
Special ports	Note when SWD is used as a GPIO	At power-up, the SWD output is pulled up high by default until the user configures it as a GPIO
Vcore	Vcore is the regulator supply output and must be connected to a 1µF capacitor to ground and is for internal circuit use only.	

2   Software checklist

Before mass production of designs based on the CW32 family of microcontrollers, the software-related configuration must be checked, as shown in the following table:

Table 2-1 Software configuration requirements

Item	Requirements	Remarks
Clock switching	The system clock should be switched in strict accordance with the user manual	See the SysClk system clock switch in the user manual for details
Clock frequency	FLASH_CR2.WAIT=0 when HCLK<=24MHz	See FLASH_CR2.WAIT function description in the user manual for details
	FLASH_CR2.WAIT=1 when 24MHz<HCLK<=48MHz	
	FLASH_CR2.WAIT=2 when 48MHz<HCLK<=72MHz	
Low power consumption	On-chip peripherals and GPIOs should be properly configured before entering low-power mode	Unused GPIOs and unpacked out GPIOs should be set to analog functionality; Clock and enable bits of unused on-chip peripherals should be turned off.
	The HCLK clock frequency must be less than or equal to 4MHz before entering DeepSleep mode	The S**32F030 automatically switches HCLK to HSI8M when it enters STOP/ STANDBY mode; Our chip requires software to switch HCLK to 4MHz and then execute the DeepSleep instruction.
	If VCx is enabled, you must wait for VCx_SR.READY flag position 1 before entering Deepsleep mode, otherwise you cannot enter Deepsleep mode.	
LSE	The OSC32_IN/OSC32_OUT pins should be set to analog functionality in the program; the LSE should be selected for high drive capability where power consumption permits.	The drive power should be in accordance with the requirements of the crystal manual
HSE	The OSC_IN/OSC_OUT pins should be set to analog functionality in the program; the HSE should be selected for high drive capability where power consumption permits.	The drive power should be in accordance with the requirements of the crystal manual

Item	Requirements	Remarks
ADC	ADC conversion speed is strongly dependent on operating voltage and reference source	See ADC conversion speed and voltage comparison table in the user manual
	If the output impedance of the ADC input signal is high, the internal voltage follower should be enabled	
BGR	Using the analog voltage comparator (VC) configuration item requires the BGR module to be turned on	See register description in the analog voltage comparator (VC) chapter of the user manual for details
RTC	When reset, the RTC configuration register value is reset; the timing value is not reset	Please refer to the RTC initialisation settings in the user manual to initialise the RTC
SWD pins	When the release version of the program does not use the SWD function, it is recommended that the SWD pins be set to the GPIO function	If the GPIO function is set, subsequent burning can only be done via the ISP protocol (6-wire connection)
Unpacked out pins	Unpacked out pins should be set to analog functionality	If the same series of MCUs has 20PIN/32PIN/48PIN, initialise the unused pins with the pin diagram for the largest package (48PIN).

3 Production checklist

Before mass production of designs based on the CW32 family of microcontrollers, attention must be paid to production-related requirements, as shown in the following table:

Table 3-1 Production checklist

Item	Requirements	Remarks
SWD pins	When programs within the MCU need to be protected: The encryption level of [LEVEL1 - LEVLE3] should be selected during burn-in.	When LEVEL2 encryption level is selected, re-burning is only possible via ISP protocol (6PIN)； When LEVEL3 encryption level is selected, the chip cannot be re-burned.
Fluxes and cleaners	No flux or cleaning residue	There is a chip burning accident caused by the customer's flux and cleaning agent residue .

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4   Revision history

Table 4-1 Document revision history

Date	Revision	Changes
May 18, 2023	Rev 1.0	Initial release.

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