LATCH UP TEST REPORT

Company ：武汉力源半导体有限公司

Address ：上海长宁区天山西路 **567** 号神州智慧大厦 **3** 楼力源

Model Name ：**CW32F030**

Date Received ：July 7, 2021

Date Tested ：July 7, 2021

TESTING LABORATORY IS APPROVEDED BY:

IECQ Certificate of Approval No.: IECQ-L DEKRA 17.0004-01 For Independent Test Laboratory According to ISO/IEC 17025

WE HEREBY CERTIFY THAT:

The test(s) shown in the attachment were conducted according to the indicating procedures. We assume full responsibility for the accuracy and completeness of these tests and vouch for the qualifications of all personnel performing them.

	Name	Signature	Date
Testing Engineer	Peter Pan	Peter Pan	2021/7/7
Approving Manager	Peng_Zhao	Peng_Zhao	2021/7/7

Note：

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.
5. The failure criteria of all ESD tests should be based on the result of parametric and functional testing conducted by the customer, which follows the statement of international standards. Thus, the judgment of the curve traces provided in this report is for reference ONLY.

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1. GENERAL INFORMATION

1.1 DESCRIPTION OF UNIT

MANUFACTURER	：武汉力源半导体有限公司
DEVICE NAME	：CW32F030
PACKAGED / PIN COUNT	：LQFP48
REFERENCE DOCUMENT	：JEDEC STANDARD NO.78E NOVEMBER 2016
TRIGGER CURRENT	：100mA~200mA,STEP:100mA (±); 300mA~700mA,STEP:100mA (-)
V SUPPLY OVER VOLTAGE TEST	：6.1V~9.1V,STEP:1.0V(+)
PULSE DURATION	：10 ms
TEST TEMPERATURE	：MAXIMA RATED TEMPERATURE @ 105 °C
SAMPLE QUANTITY	：6 pcs
FAILURE CRITERIA	：If absolute Inom is < 25 mA, then absolute Inom + 10mA is used; Or If absolute Inom is > 25 mA, then > 1.4X absolute Inom is used;

2. LATCH UP TEST

2.1 TEST EQUIPMENT

Test Equipment	Equipment S/N	Calibration Date:	Recommended Due Date:
KEYTEK ZAPMASTER MK2 768	1409189	March 23, 2021	March 22, 2022

2.2 LABORATORY AMBIENCE CONDITION

Temperature：25°C$^{+3°C}_{-5°C}$

Relative humidity：55%±10% (RH)

2.3 REFERENCE DOCUMENT

The test is based on JEDEC STANDARD NO.78E NOVEMBER 2016

2.4 TEST CONDITION

I Trigger

Over Voltage Test

2.5 SUMMARY OF TEST

Trigger Mode	Test Pin	Sample Quantity	Tested Result	V or I Limits	I Trigger : Class ⅡA
I Trigger (+)	IO6.05V	3	PASS +200mA	+9.075V	CLASS Ⅰ For Latch-up test at room temperature Class Ⅰ A : Positive I-Test : ≧ 100mA Negative I-Test : ≧ 100mA Overvoltage Test : 1.5 x VDD or MSV, whichever is less Class Ⅰ B : If immunity level A cannot be achieved CLASS Ⅱ For Latch-up test at maximum-rate ambient temperature Class Ⅱ A : Positive I-Test : ≧ 100mA Negative I-Test : ≧ 100mA Overvoltage Test : 1.5 x VDD or MSV, whichever is less Class Ⅱ B : If immunity level A cannot be achieved
I Trigger (-)	IO6.05V		PASS -200mA	-3.025V	
Over Volt Test V_{supply}	VDD6.05V		PASS + 9.1V	+600mA	
I Trigger (-)	IO6.05V	3	PASS -700mA	-3.025V	

IO6.05V	2~7,10~22,25~46
VDD6.05V	1,9,24,48
GND	8,23,47

2.6 CONTENTS OF TEST

I Trigger (Positive)							
Tested Pin	Sample No. & Failed current (mA)			Tested Pin	Sample No. & Failed current (mA)		
	#L7	#L8	#L9		#L7	#L8	#L9
2	PASS+200mA	PASS+200mA	PASS+200mA	27	PASS+200mA	PASS+200mA	PASS+200mA
3	PASS+200mA	PASS+200mA	PASS+200mA	28	PASS+200mA	PASS+200mA	PASS+200mA
4	PASS+200mA	PASS+200mA	PASS+200mA	29	PASS+200mA	PASS+200mA	PASS+200mA
5	PASS+200mA	PASS+200mA	PASS+200mA	30	PASS+200mA	PASS+200mA	PASS+200mA
6	PASS+200mA	PASS+200mA	PASS+200mA	31	PASS+200mA	PASS+200mA	PASS+200mA
7	PASS+200mA	PASS+200mA	PASS+200mA	32	PASS+200mA	PASS+200mA	PASS+200mA
10	PASS+200mA	PASS+200mA	PASS+200mA	33	PASS+200mA	PASS+200mA	PASS+200mA
11	PASS+200mA	PASS+200mA	PASS+200mA	34	PASS+200mA	PASS+200mA	PASS+200mA
12	PASS+200mA	PASS+200mA	PASS+200mA	35	PASS+200mA	PASS+200mA	PASS+200mA
13	PASS+200mA	PASS+200mA	PASS+200mA	36	PASS+200mA	PASS+200mA	PASS+200mA
14	PASS+200mA	PASS+200mA	PASS+200mA	37	PASS+200mA	PASS+200mA	PASS+200mA
15	PASS+200mA	PASS+200mA	PASS+200mA	38	PASS+200mA	PASS+200mA	PASS+200mA
16	PASS+200mA	PASS+200mA	PASS+200mA	39	PASS+200mA	PASS+200mA	PASS+200mA
17	PASS+200mA	PASS+200mA	PASS+200mA	40	PASS+200mA	PASS+200mA	PASS+200mA
18	PASS+200mA	PASS+200mA	PASS+200mA	41	PASS+200mA	PASS+200mA	PASS+200mA
19	PASS+200mA	PASS+200mA	PASS+200mA	42	PASS+200mA	PASS+200mA	PASS+200mA
20	PASS+200mA	PASS+200mA	PASS+200mA	43	PASS+200mA	PASS+200mA	PASS+200mA
21	PASS+200mA	PASS+200mA	PASS+200mA	44	PASS+200mA	PASS+200mA	PASS+200mA
22	PASS+200mA	PASS+200mA	PASS+200mA	45	PASS+200mA	PASS+200mA	PASS+200mA
25	PASS+200mA	PASS+200mA	PASS+200mA	46	PASS+200mA	PASS+200mA	PASS+200mA
26	PASS+200mA	PASS+200mA	PASS+200mA	----	----	----	----

I Trigger (Negative)							
Tested Pin	Sample No. & Failed current (mA)			Tested Pin	Sample No. & Failed current (mA)		
	#L7	#L8	#L9		#L7	#L8	#L9
2	PASS-200mA	PASS-200mA	PASS-200mA	27	PASS-200mA	PASS-200mA	PASS-200mA
3	PASS-200mA	PASS-200mA	PASS-200mA	28	PASS-200mA	PASS-200mA	PASS-200mA
4	PASS-200mA	PASS-200mA	PASS-200mA	29	PASS-200mA	PASS-200mA	PASS-200mA
5	PASS-200mA	PASS-200mA	PASS-200mA	30	PASS-200mA	PASS-200mA	PASS-200mA
6	PASS-200mA	PASS-200mA	PASS-200mA	31	PASS-200mA	PASS-200mA	PASS-200mA
7	PASS-200mA	PASS-200mA	PASS-200mA	32	PASS-200mA	PASS-200mA	PASS-200mA
10	PASS-200mA	PASS-200mA	PASS-200mA	33	PASS-200mA	PASS-200mA	PASS-200mA
11	PASS-200mA	PASS-200mA	PASS-200mA	34	PASS-200mA	PASS-200mA	PASS-200mA
12	PASS-200mA	PASS-200mA	PASS-200mA	35	PASS-200mA	PASS-200mA	PASS-200mA
13	PASS-200mA	PASS-200mA	PASS-200mA	36	PASS-200mA	PASS-200mA	PASS-200mA
14	PASS-200mA	PASS-200mA	PASS-200mA	37	PASS-200mA	PASS-200mA	PASS-200mA
15	PASS-200mA	PASS-200mA	PASS-200mA	38	PASS-200mA	PASS-200mA	PASS-200mA
16	PASS-200mA	PASS-200mA	PASS-200mA	39	PASS-200mA	PASS-200mA	PASS-200mA
17	PASS-200mA	PASS-200mA	PASS-200mA	40	PASS-200mA	PASS-200mA	PASS-200mA
18	PASS-200mA	PASS-200mA	PASS-200mA	41	PASS-200mA	PASS-200mA	PASS-200mA
19	PASS-200mA	PASS-200mA	PASS-200mA	42	PASS-200mA	PASS-200mA	PASS-200mA
20	PASS-200mA	PASS-200mA	PASS-200mA	43	PASS-200mA	PASS-200mA	PASS-200mA
21	PASS-200mA	PASS-200mA	PASS-200mA	44	PASS-200mA	PASS-200mA	PASS-200mA
22	PASS-200mA	PASS-200mA	PASS-200mA	45	PASS-200mA	PASS-200mA	PASS-200mA
25	PASS-200mA	PASS-200mA	PASS-200mA	46	PASS-200mA	PASS-200mA	PASS-200mA
26	PASS-200mA	PASS-200mA	PASS-200mA	----	----	----	----

I Trigger (Negative)							
Tested Pin	Sample No. & Failed current (mA)			Tested Pin	Sample No. & Failed current (mA)		
	#L10	#L11	#L12		#L10	#L11	#L12
2	PASS-700mA	PASS-700mA	PASS-700mA	27	PASS-700mA	PASS-700mA	PASS-700mA
3	PASS-700mA	PASS-700mA	PASS-700mA	28	PASS-700mA	PASS-700mA	PASS-700mA
4	PASS-700mA	PASS-700mA	PASS-700mA	29	PASS-700mA	PASS-700mA	PASS-700mA
5	PASS-700mA	PASS-700mA	PASS-700mA	30	PASS-700mA	PASS-700mA	PASS-700mA
6	PASS-700mA	PASS-700mA	PASS-700mA	31	PASS-700mA	PASS-700mA	PASS-700mA
7	PASS-700mA	PASS-700mA	PASS-700mA	32	PASS-700mA	PASS-700mA	PASS-700mA
10	PASS-700mA	PASS-700mA	PASS-700mA	33	PASS-700mA	PASS-700mA	PASS-700mA
11	PASS-700mA	PASS-700mA	PASS-700mA	34	PASS-700mA	PASS-700mA	PASS-700mA
12	PASS-700mA	PASS-700mA	PASS-700mA	35	PASS-700mA	PASS-700mA	PASS-700mA
13	PASS-700mA	PASS-700mA	PASS-700mA	36	PASS-700mA	PASS-700mA	PASS-700mA
14	PASS-700mA	PASS-700mA	PASS-700mA	37	PASS-700mA	PASS-700mA	PASS-700mA
15	PASS-700mA	PASS-700mA	PASS-700mA	38	PASS-700mA	PASS-700mA	PASS-700mA
16	PASS-700mA	PASS-700mA	PASS-700mA	39	PASS-700mA	PASS-700mA	PASS-700mA
17	PASS-700mA	PASS-700mA	PASS-700mA	40	PASS-700mA	PASS-700mA	PASS-700mA
18	PASS-700mA	PASS-700mA	PASS-700mA	41	PASS-700mA	PASS-700mA	PASS-700mA
19	PASS-700mA	PASS-700mA	PASS-700mA	42	PASS-700mA	PASS-700mA	PASS-700mA
20	PASS-700mA	PASS-700mA	PASS-700mA	43	PASS-700mA	PASS-700mA	PASS-700mA
21	PASS-700mA	PASS-700mA	PASS-700mA	44	PASS-700mA	PASS-700mA	PASS-700mA
22	PASS-700mA	PASS-700mA	PASS-700mA	45	PASS-700mA	PASS-700mA	PASS-700mA
25	PASS-700mA	PASS-700mA	PASS-700mA	46	PASS-700mA	PASS-700mA	PASS-700mA
26	PASS-700mA	PASS-700mA	PASS-700mA	----	----	----	----

Over Voltage Test for V_{supply}			
Tested Pin	Sample No. & Failed Volt (V)		
	#L7	#L8	#L9
1	PASS	PASS	PASS
9	PASS	PASS	PASS
24	PASS	PASS	PASS
48	PASS	PASS	PASS