

ESD (MACHINE MODE) TEST REPORT

Company : 武汉力源半导体有限公司
Address : 上海长宁区天山西路 567 号神州智慧大厦 3 楼力源
Model Name : CW32F030
Date Received : July 7, 2021
Date Tested : July 7, 2021

TESTING LABORATORY IS APPROVED BY:

IECQ Certificate of Approval No.: IECQ-L DEKRA 17.0004-01 For Independent Test Laboratory
According to ISO/IEC 17025

WE HEREBY CERTIFY THAT:

The test(s) shown in the attachment were conducted according to the indicating procedures.
We assume full responsibility for the accuracy and completeness of these tests and vouch
for the qualifications of all personnel performing them.

	Name	Signature	Date
Testing Engineer	Peter Pan	<i>Peter Pan</i>	2021/7/7
Approving Manager	Peng_Zhao	<i>Peng Zhao</i>	2021/7/7

Note :

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.
5. The failure criteria of all ESD tests should be based on the result of parametric and functional testing conducted by the customer, which follows the statement of international standards. Thus, the judgment of the curve traces provided in this report is for reference ONLY.



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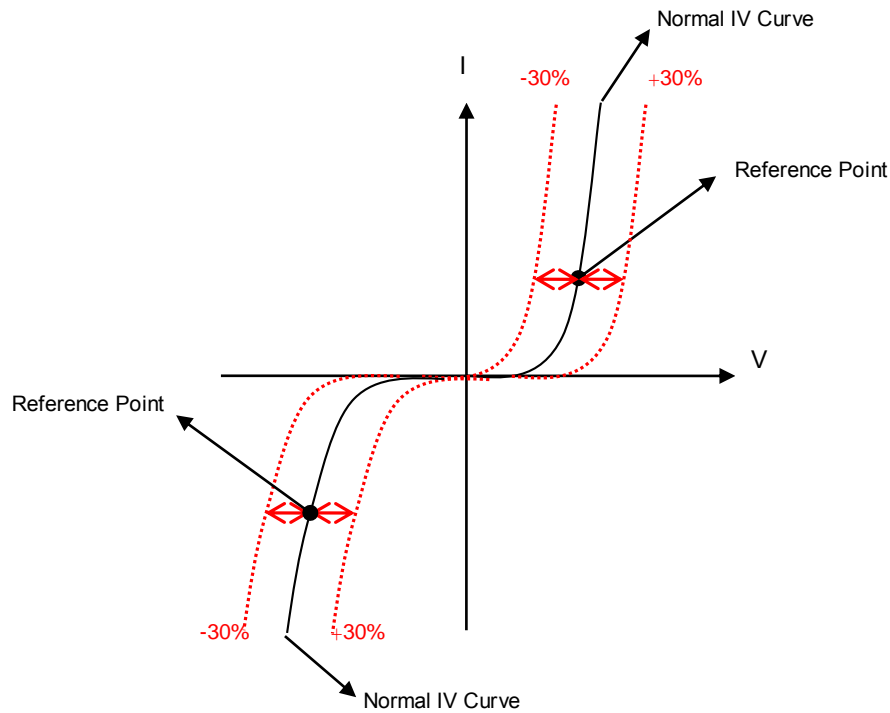
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1. GENERAL INFORMATION

1.1 DESCRIPTION OF UNIT

MANUFACTURER : 武汉力源半导体有限公司
DEVICE NAME : CW32F030
PACKAGED / PIN COUNT : LQFP48
REFERENCE DOCUMENT : JEDEC EIA/JESD22-A115C Zap 1 pulse(s), Interval: 0.5 Sec.
TEST VOLTAGE : 400V~FAIL,STEP:100V(±)
SAMPLE QUANTITY : 3 pcs
FAILURE CRITERIA : ±30% voltage shift at reference point before/after zapping
(Reference Only)

※Failure Judgment: Voltage shift over ±30% at reference point.



2. ESD (MACHINE MODE) TEST

2.1 TEST EQUIPMENT

Test Equipment	Equipment S/N	Calibration Date:	Recommended Due Date:
KEYTEK ZAPMASTER MK2 768	1409189	March 23, 2021	March 22, 2022

2.2 LABORATORY AMBIENCE CONDITION

Temperature : 25°C^{+3°C}_{-5°C}

Relative humidity : 55%±10% (RH)

2.3 REFERENCE DOCUMENT

The test is based on JEDEC EIA/JESD22-A115C

2.4 TEST CONDITION

ALL OTHER PINS TO VSS+VSSA (+/-)
400V~FAIL,STEP:100V
ALL OTHER PINS TO VDD (+/-)
400V~FAIL,STEP:100V
ALL OTHER PINS TO VDDA (+/-)
400V~FAIL,STEP:100V
IOGroup01 TO IOGroup01 (+/-)
400V~FAIL,STEP:100V

2.5 SUMMARY OF TEST

Test Model : MM	ESD Sensitivity Passed : <u>+/-400V</u>		JEDEC-STD Classification Class : <u>C</u>
Test condition	Sample Quantity	Passed Volts	Class A : < 200V. Class B : \geq 200V , < 400V Class C : \geq 400V
ALL OTHER PINS TO VSS+VSSA (+/-) 400V~FAIL,STEP:100V ALL OTHER PINS TO VDD (+/-) 400V~FAIL,STEP:100V ALL OTHER PINS TO VDDA (+/-) 400V~FAIL,STEP:100V IOGroup01 TO IOGroup01 (+/-) 400V~FAIL,STEP:100V	3	+/-400V	

Group Set Pin List

IOGroup01 2-7,10-22,25-46

VDD 1,24,48

VDDA 9

VSS 23,47

VSSA 8

2.6 CONTENTS OF TEST

No.	1		
	ALL OTHER PINS TO VSS+VSSA (+/-) 400V~FAIL,STEP:100V ALL OTHER PINS TO VDD (+/-) 400V~FAIL,STEP:100V ALL OTHER PINS TO VDDB (+/-) 400V~FAIL,STEP:100V IOGroup01 TO IOGroup01 (+/-) 400V~FAIL,STEP:100V		
Tested Pins	Sample No. & Failed Volt		
	#M04	#M05	#M06
1	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
2	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
3	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
4	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
5	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
6	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
7	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
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23	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
24	FAIL(+/-500V)	FAIL(+/-500V)	FAIL(+/-500V)
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26	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
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41	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)



42	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
43	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
44	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
45	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
46	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
47	PASS(+/-500V)	PASS(+/-500V)	PASS(+/-500V)
48	FAIL(+/-500V)	FAIL(+/-500V)	FAIL(+/-500V)